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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10065694	11/11/2002	714	718	2133	<i>Decker</i>

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****CONTINUING DATA VERIFIED:**

**** FOREIGN APPLICATIONS VERIFIED:**

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no			ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no			BUR920010195
Verified and Acknowledged Examiners's initials			
TITLE : Method for testing embedded DRAM arrays			

U S DEPT OF COMM /PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs.Drwg.
Primary Examiner		Print Fig.	
PREPARED FOR ISSUE		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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